Learning while Designing a Counter/Timer

RF Seminar

Paraphrasing Pippi Langkous:
I've never designed a counter so I think I know how to do it.

Content

- Context
- Initial ambition
- Prototyping steps
- HW flexibility
- First HW : CPLD problems
- Second HW : Timing problems
- Second HW : Component problems
- Second HW : System design problems
- Beta testing feedback
- Third HW: Robustness problems
- Fourth HW: Final performance (?)
- Learnings

Disclaimer:
This presentation describes a limited set of simplified HW related problems.
The reality is much more complex.

Context

- Who am I?
  - Erik Kaashoek, PD0EK.
  - Wanted to do something with electronics/software after retiring
  - Got my license 4 days after retiring so I had a subject to work on.
  - Did not have any RX/TX (buying is boring) so started to build one.
  - As I had no test equipment, I started designing and building my own.

- What test equipment did I design?
  - Various measurement tools for own use (VNA, SA)
  - tinySA Basic: 0-960 MHz spectrum analyzer and RF generator
  - tinySA Ultra: 0-5.3 GHz spectrum analyzer and RF generator
  - tinyPFA: Very accurate 1-250 MHz frequency and phase analyzer
  - tinySA Ultra +: 0-7.3 GHz spectrum analyzer and RF generator.

- Why design a counter/timer?
  - I needed one (tinyPFA can not measure low frequencies or time)
  - It is (was) a fun side project next to all the tinySA/tinyPFA work
  - Various tinySA resellers asked for such a product

Initial Design Ambition

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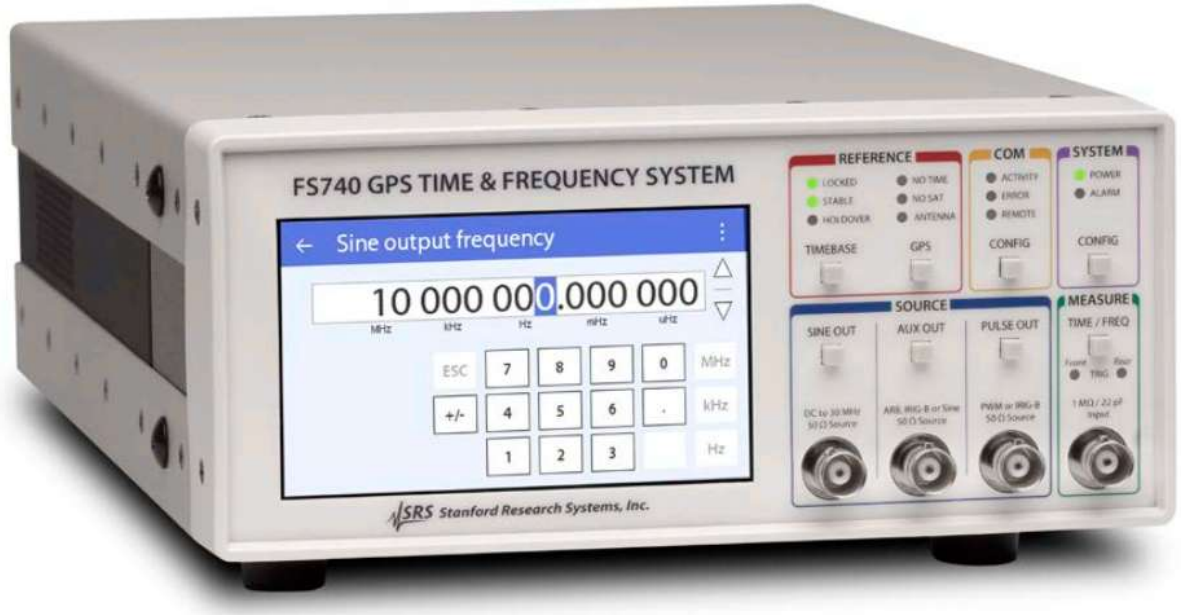
- Difference with available cheap counters:
  - Gapless, e.g. ADEV measurement capable
  - Time stamping and Phase measurement
  - Two fully independent inputs for simultaneous measurement of 3 clocks
  - DC coupled inputs allowing low input frequencies
  - Portable, battery operated, no OCXO
  - Built in GPSDO, external reference possible
- Target performance:
  - Measures 0.1 Hz to 100 MHz with ADEV 1e-9 @ 1 s
    - Reciprocal counter
  - 10 MHz GPSDO with ADEV 1e-9 @ 1 s – 100 s
    - Typical good TCXO performance

Inspiration: FS740 from SRS



- Dual timer/counter
- Built-in GPSDO
- Flexible outputs
- Accuracy: 1e-12/s
- UTC timestamping
- SCPI support
- Starts at $4800

First counter prototype

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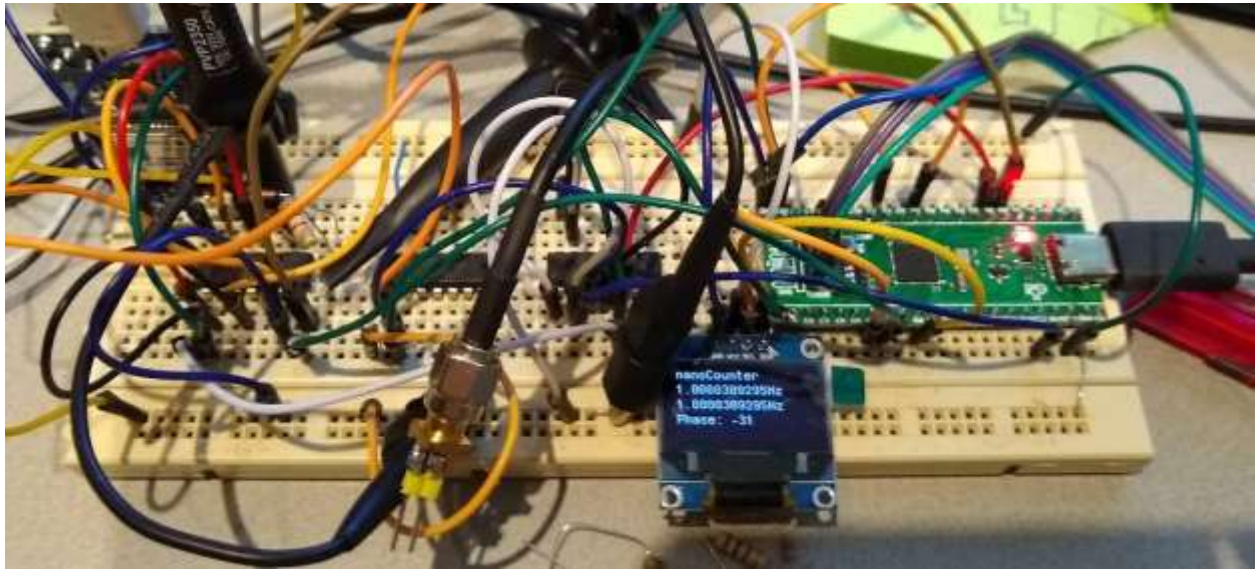
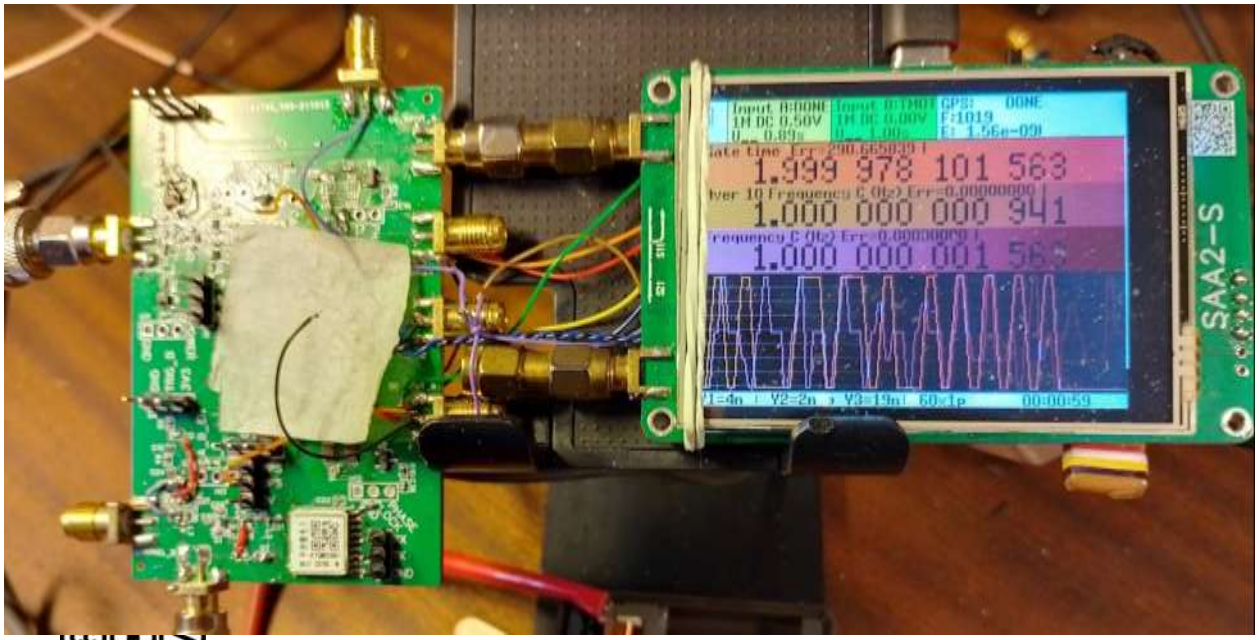
- Started August 2021, Fully operational October 2021
- Textbook two channel reciprocal counter, digital inputs
- HW: STM32F303 + 3 logic IC’s
- ADEV 1e-9 @ 1 s
- Conclusion after some quick testing: Counters are simple



Second counter prototype

- Two channel reciprocal counter + GPSDO
- HW: STM32F303 + analog and logic IC's + GPS + TCXO
- Analog front-end with trigger level between 0-3.5 V
- GPSDO ADEV 1e-9 @ 1 s – 100 s
- Conclusion : Almost full functional, still easy



Improving Design flexibility

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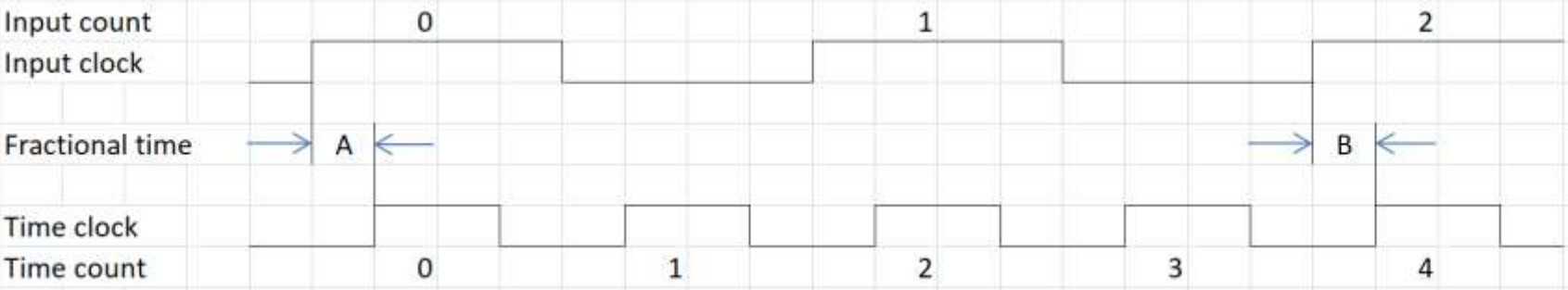
- Functionality of counter still being extended
  - External gating, Time interval, Counting
- SW flexibility great but HW very inflexible
  - Any change requires soldering wires and/or getting new components
- Unproven functionality mainly in logic IC's
- Solution: Replace all logic IC's by one CPLD

Improving Accuracy

- As everything was going well, aim for next level of performance
- Time measurement accuracy of 4 ns limited by time counter maximum clock speed of 240 MHz
- Add fractional time measurement with 40 ps accuracy. This should improve time accuracy with a factor 100 (1e-11)



Input Freqeuency = (Input count) / (Time count * Time period + Fractional time A - Fractional time B)

Time period = 4 ns

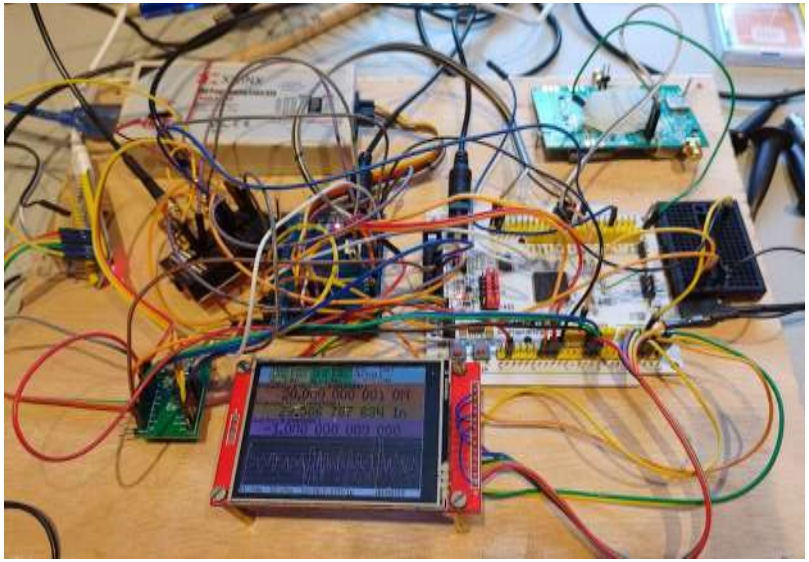
Fractional time A = 1 ns

Fractional time B = 1 ns

Input Frequency = 125 MHz

Third counter prototype

- Replace all logic IC's by one CPLD for design flexibility
- Added fractional time measurement using TDC's, ADEV goal: 1e-11 @ 1 s gate time.
- Added pre-scaler for measurements up to 6 GHz
- Full functional HW created to test full functional SW
- Stability problems and ADEV not so good due to long wires.
- Fully integrated PCB should work "out of the box" with very good performance
- Next step: PCB design
- Build fully integrated model
- Launch before end 2023?



First complete HW model

(July 2023)

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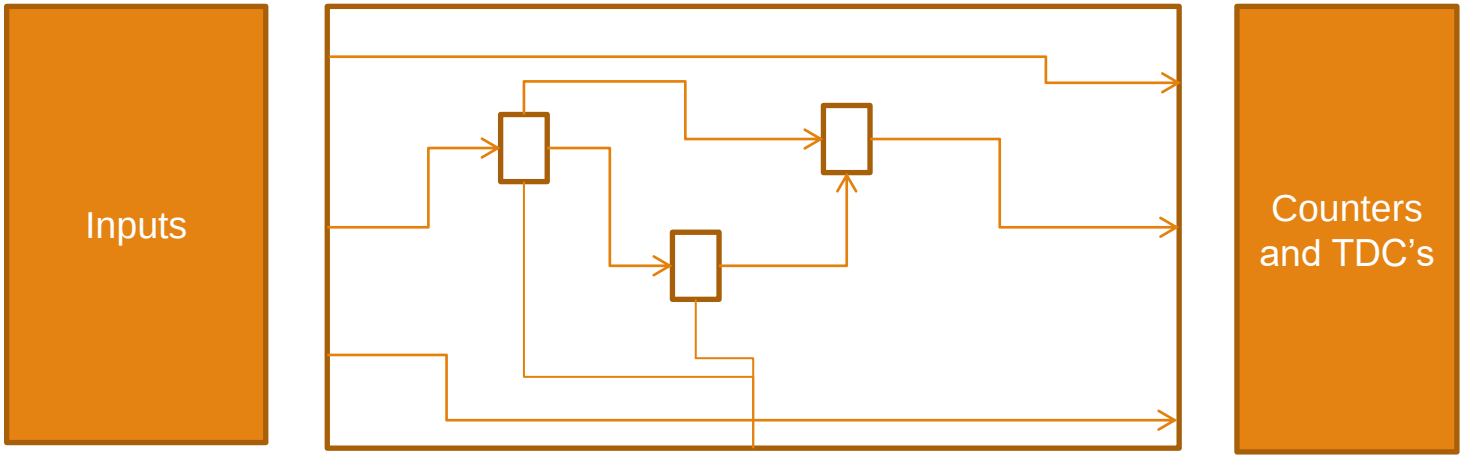
- PCB: RF design using 4 layers with 2 ground planes and separate voltage regulators per function.
- HW/SW fully functional at first startup
- However, performance not as expected.

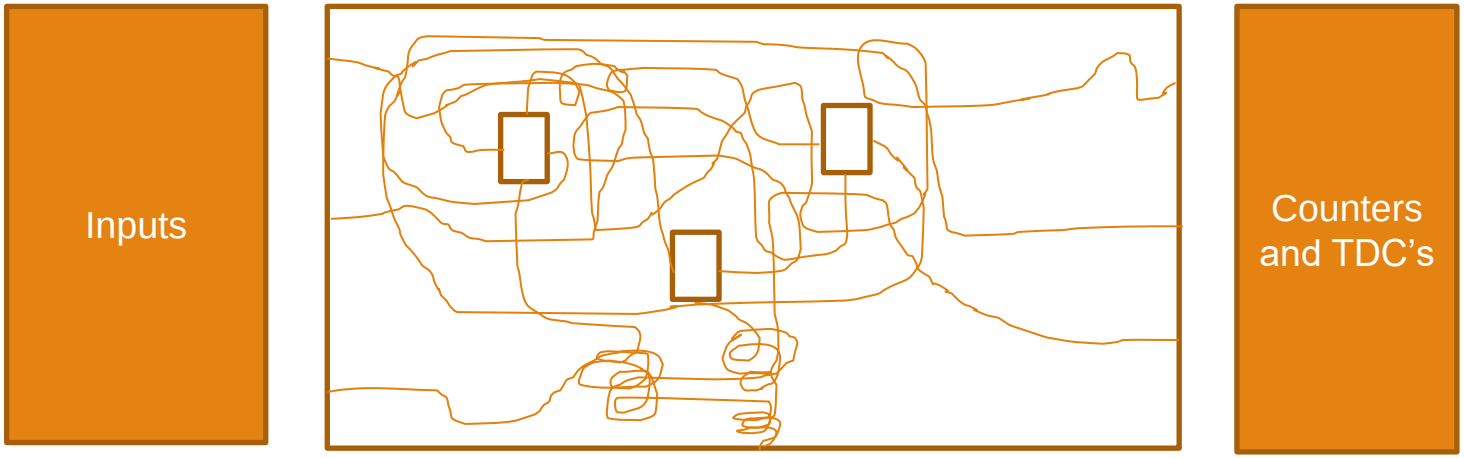
CPLD expectation

- All logic inside a single CPLD
- Various signals routed through CPLD to simplify layout
- CPLD design tools suggest a nice clear abstraction with perfect logical signals
- Actual performance suggested a lot of imperfection.



CPLD reality

- At high frequencies everything becomes analog
  - CPLD max frequency is 350 MHz, TDC resolution equals 25 GHz
- Various reasons for coupling between signals
  - Actual routing in the CPLD is complex/random
  - Used CPLD package rather large
  - Small number of ground pins with high inductance cause ground coupling
- All signals routed into/through CPLD become coupled.



CPLD lessons

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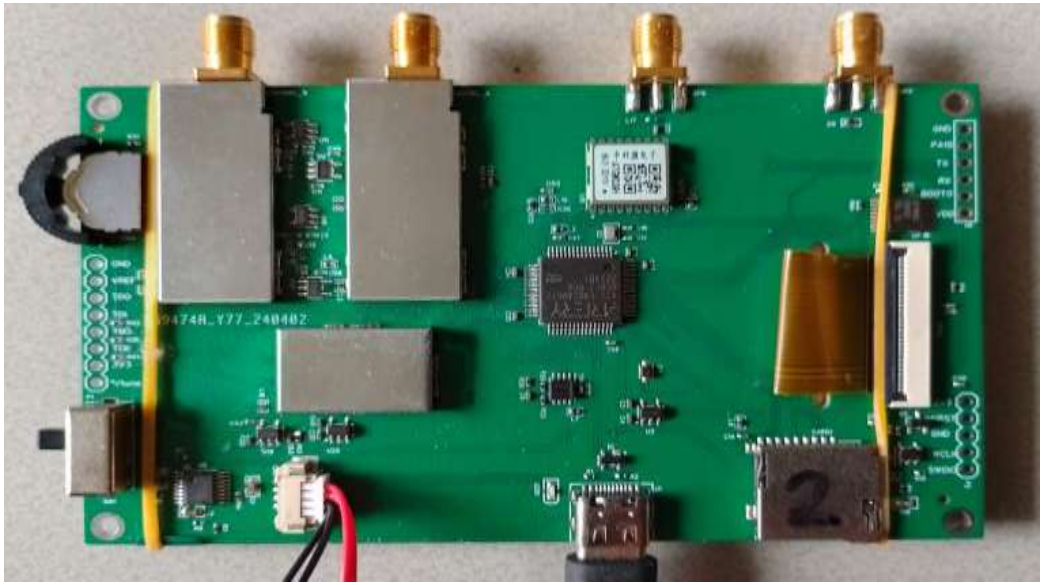
- Avoid edge collisions
  - Use one CPLDs per related group of signals
  - Avoid multiple clock domains in one CPLD
  - Don’t route signals through CPLD
- Use small footprint CPLD’s with ground pad to reduce internal wire length and reduce grounding coupling.
- With new CPLD’s performance should be good

2nd HW model

(Feb 2024)

- Each input has its own small CPLD under the shield
- TDC's close to inputs also under the shield
- Performance disappointing
  - ADEV improved a bit for some input frequencies but still not good, also time stamping bad.
- Needed to debug the counters



How to debug a counter?

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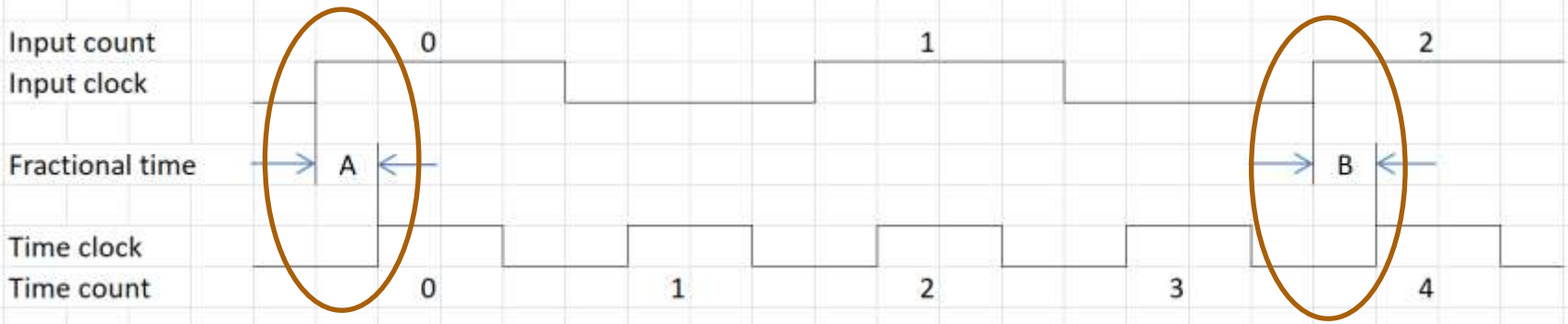
- Time Counters run at 240 MHz, impossible to probe, any disturbance causes miscounts.
- Highly optimized data collection and calculation already generates 50 % MCU load
- It is possible to store raw data for 0.4 s
- Often 10’s of seconds with good performance and suddenly very bad performance.
- Need criteria to selectively store data for analysis

Reciprocal Interpolating frequency measurement

- Textbook approach: 3 measurements per gate trigger
  - Input trigger count
  - Time clock count
  - Fractional time



Input Freqeuency = (Input count) / (Time count * Time period + Fractional time A - Fractional time B)

Time period = 4 ns

Fractional time A = 1 ns

Fractional time B = 1 ns

Input Frequency = 125 MHz

Detecting and logging errors

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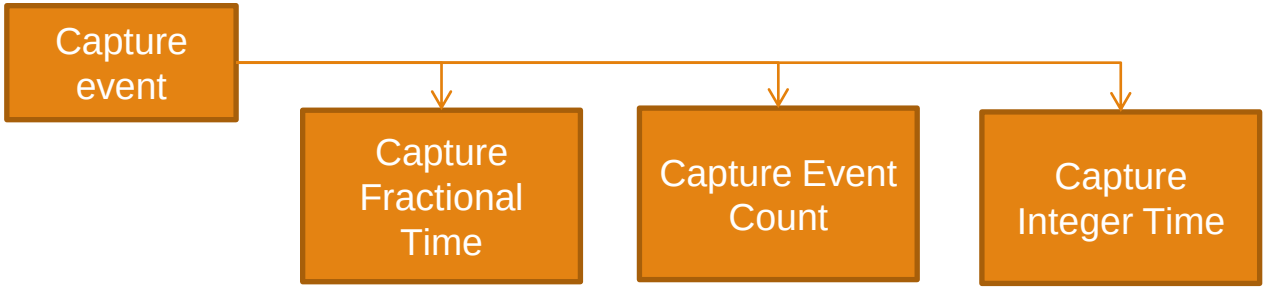
- Use stable input frequency
- Measurement every 0.1 ms
  - Count and time vary
  - Frequency is “constant” with noise
- System learns input frequency
- Large frequency deviations signals error and triggers data logging
- Also log measurements before and after error to see what changed
- Collect and analyze many hours of data to find cause of errors

count	time	fraction	fract time	freq
983	23592	0.4575	23592.010	9999996
1000	24000	0.4850	23999.973	10000011
1000	24000	0.4775	24000.008	9999997
1058	25392	0.5025	25391.975	10000010
942	22608	0.5225	22607.980	10000009
1000	24000	0.5450	23999.978	10000009
1000	24000	0.5350	24000.010	9999996
1000	24000	0.5575	23999.978	10000009
1000	24000	0.5600	23999.998	10000001
1000	24000	0.5725	23999.988	10000005
1000	24000	0.5750	23999.998	10000001
1000	24000	0.5975	23999.978	10000009
1000	24000	0.5900	24000.008	9999997
1000	24000	0.6025	23999.988	10000005
1000	24000	0.5900	24000.013	9999995
1000	24000	0.6075	23999.983	10000007
1000	24000	0.6350	23999.973	10000011
1000	24000	0.6325	24000.003	9999999
1000	24000	0.6400	23999.993	10000003
1000	24000	0.6550	23999.985	10000007
1000	24000	0.6825	23999.973	10000011
1000	24000	0.6700	24000.013	9999995
1000	24000	0.6875	23999.983	10000007
1000	24000	0.7050	23999.983	10000007
1000	24000	0.7225	23999.983	10000007
1000	24000	0.7175	24000.005	9999998
1000	24000	0.7275	23999.990	10000004

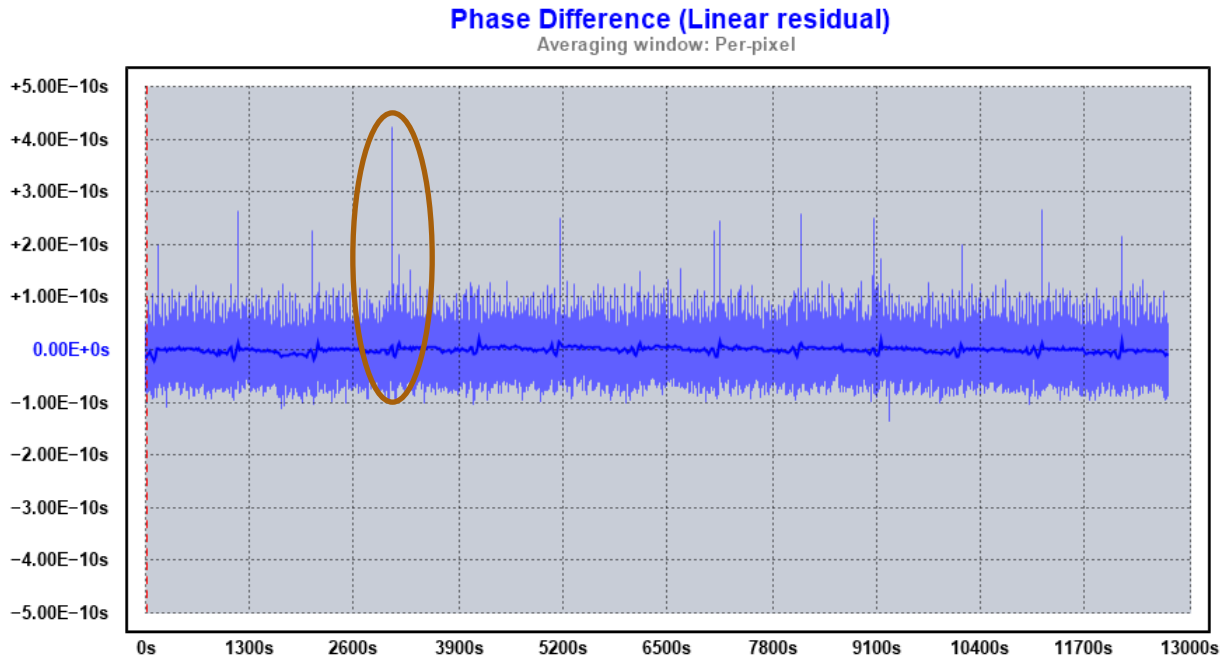
What could cause capture errors?

- Capture event triggers 3 simultaneous captures in two IC's
  - Event count and Time count capture triggers have separate IC inputs
  - Event count and Time count capture triggers are re-clocked with 240 MHz system clock
  - Fractional time capture in separate IC
- No possible error in capture of event count as capture event is synced with trigger
- But 240 MHz system clock is not locked to input event clock causing the Time count capture to "wander" versus the 240 MHz system clock
- As a result +/- 1 count errors possible in Integer Time capture.
  - Causes 4 ns time measurement errors
  - Impossible to avoid in counter HW



Capture errors (2)

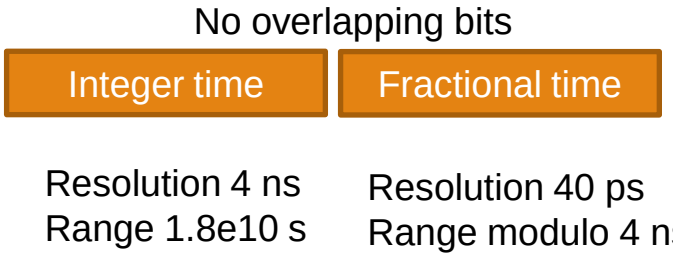
- Most visible when doing time stamping as infrequent large deviation
- Outlier filter can remove these when measuring frequency or phase above 1 MHz. No solution for low frequencies.
- Can severely degrade the performance at low frequencies.



Trace	Notes	Input Freq	Sample Interval	Phase at 21s	Acquired	Instrument
timestamp 10 MHz in		10 MHz	0.100 s	6.20E−8s	127295 pts	tinyGTC

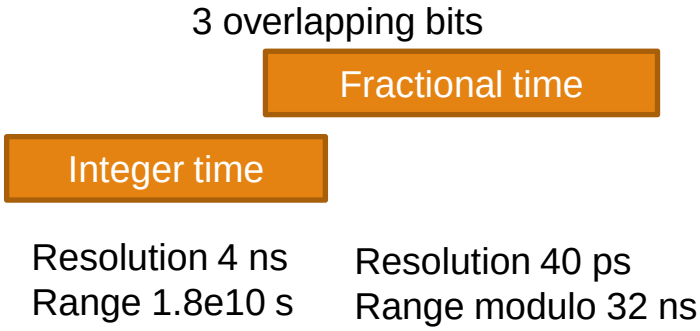
Textbook design with separate integer and fractional time measurement causes +/- 1 count errors

- Fractional time range 0 to 3.999 ns
- Impossible to detect integer count errors
- Total time = Integer time + fractional time
- Uncertainty: +/- 1 integer count (4 ns)



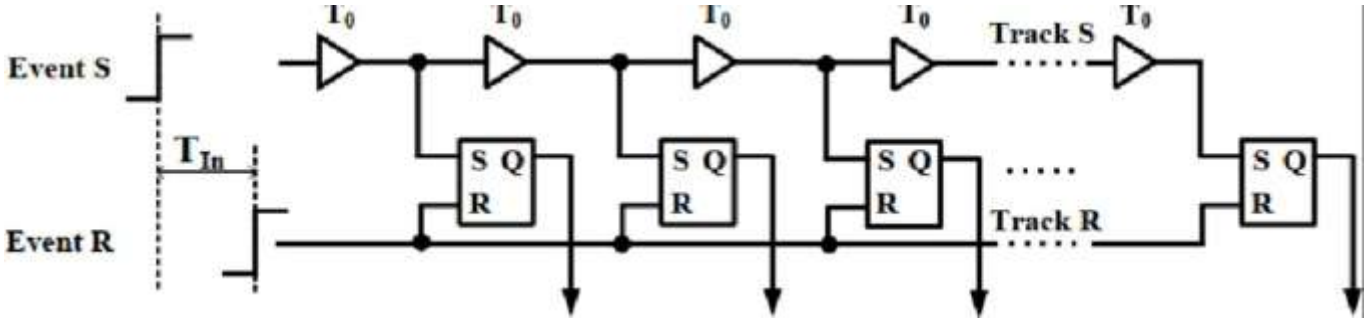
New design uses overlapping time to eliminate +/- 1 count errors

- Fractional time range 0 to 31.999 ns
- Inconsistency between (integer time modulo 8) and 3 highest bits of fractional time signals count error
- Total time= Integer time + fractional time + error correction
- Uncertainty: +/- 1 fractional bit (40 ps)



TDC performance check

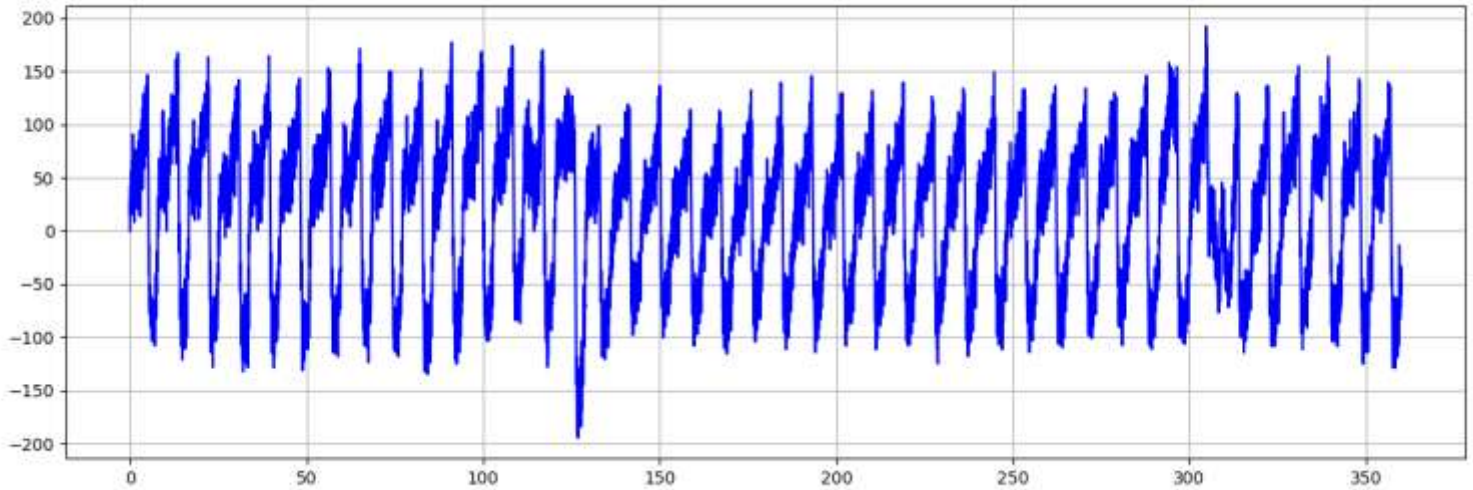
- With +/- 1 count error removed no more large deviations.
- Remaining measurement noise had too much “structure”
- TDC step size/linearity depends on gate delays



- TDC non linearity? How to measure???
  - TDC range 100 ns, step 40 ps.
  - Scanning whole TDC range requires pulse that varies between 0 and 100 ns in below 40 ps steps.
    - Impossible to generate.
  - Use Vernier method instead

TDC performance below expectations

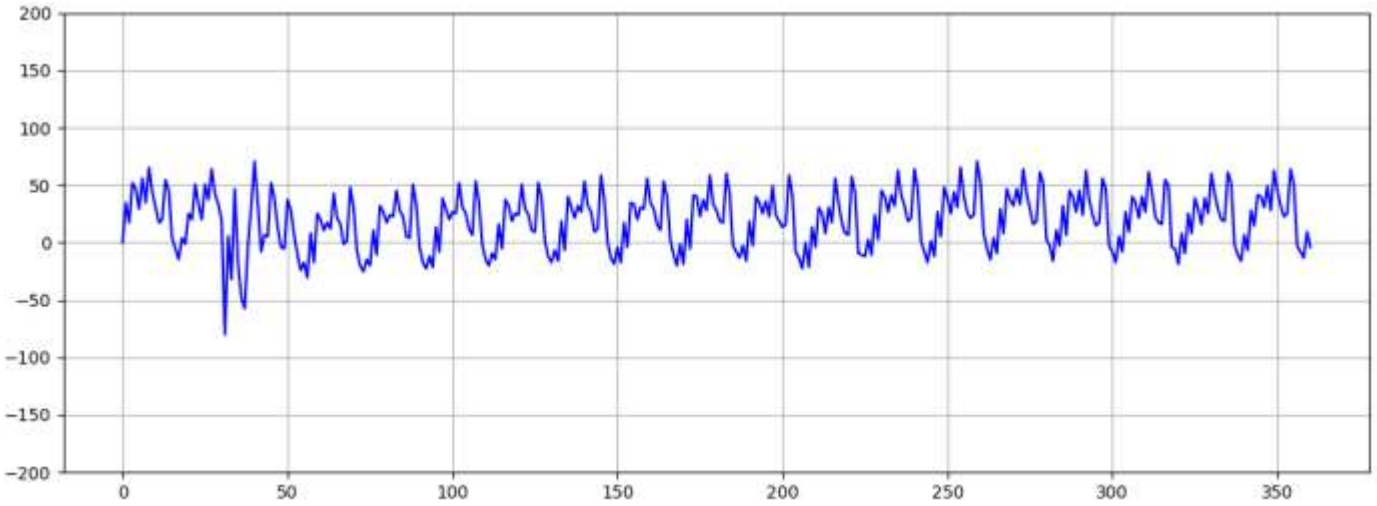
- Vernier test signal
  - Measure the **linear residue of the unwrapped phase difference** of two slightly different frequencies (10 MHz + 10.000000001 MHz to create 1000 s period)
- All TDC's appeared to have a very visible non-linearity with exactly 54 buckets period (vert. scale +/- 200 ps). Non linearity max 400 ps.



- Shape, amplitude and phase differs per TDC and changes with temperature so no compensation possible
- TDC manufacturer confirmed problem is inside the TDC.
- Switched to different TDC with better linearity

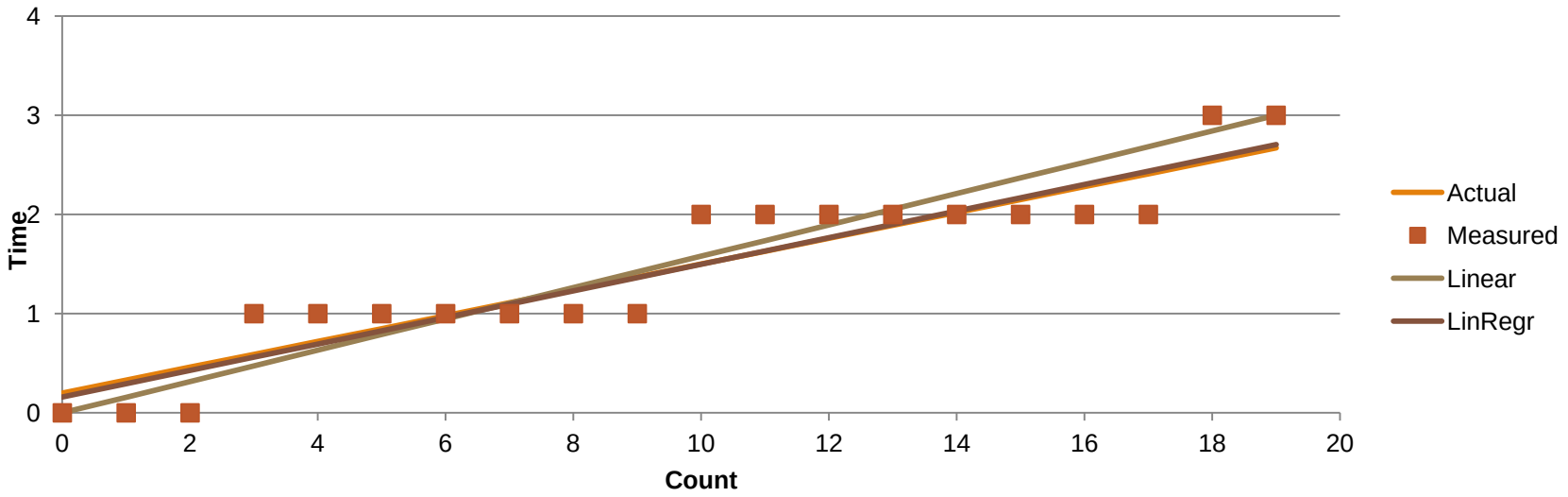
New TDC performance

- Much less structure in the noise
  - Same vertical scale as previous plot
  - One TDC step is 40 ps.
  - Data is average over many measurements



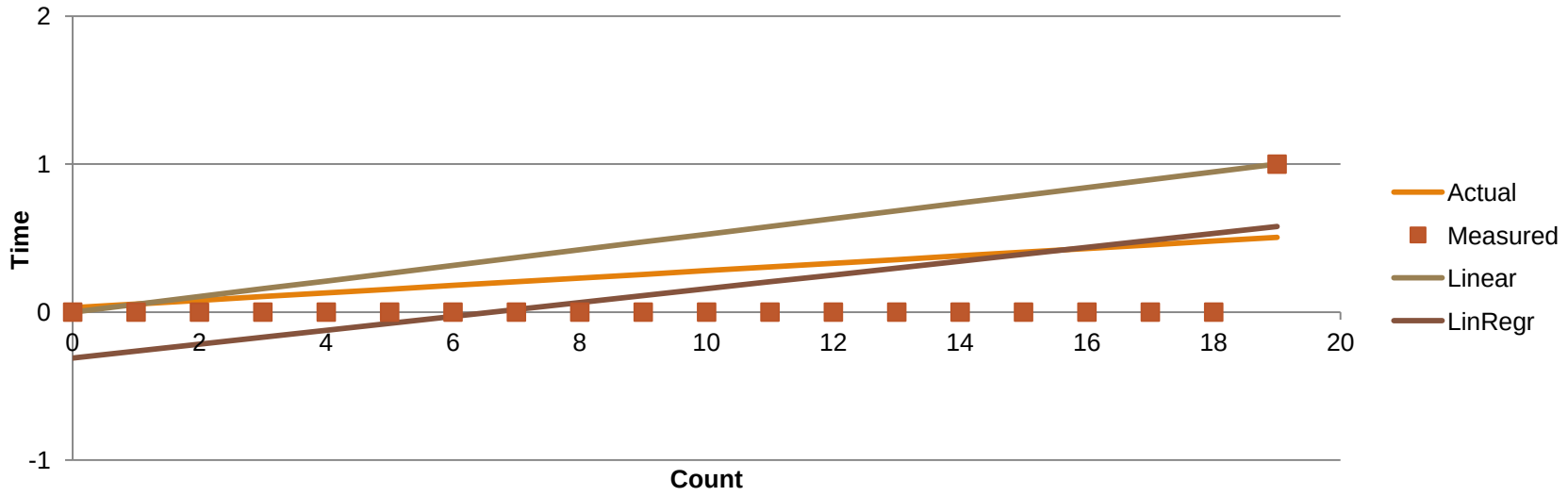
Interpolating counter limitation

- Time has limited resolution (40 ps)
- Linear regression improves frequency accuracy beyond this resolution



Interpolation problem

- If input frequency is close to reference frequency most time measurements provide no information
- As a result the Linear Regression no longer improves frequency accuracy



Solving the “close to reference” problem (1)

- Problem:
  - Performance very good, except when measuring close to internal reference clock
  - Internal reference clock was 10 MHz
- Traditional Solution:
  - Add dithering and oversampling like in ADC
  - Down sampling to actual input rate removes noise from dithering and gives accuracy beyond measurement resolution.
- New problem:
  - Unclear how to do dithering on ps scale
  - Dithering destroys the single shot accuracy so for time measurement dithering must be disabled
  - One counter must be able to do simultaneously single shot time measurements while also doing regression enhanced frequency measurements

Solving the “close to reference” problem (2)

- Problem:
  - How to add “dithering” without destroying single shot time measurement?
- Solution:
  - Add a flexible clock generator that can generate “any” internal reference clock
  - Set the reference clock to a uncommon value, away from 10 MHz
  - Problem area is less the 1 Hz wide
- Adding this flexible clock generator enabled two flexible clocks outputs instead of single 10 MHz clock output
  - OUT: 0.1 Hz – 100 MHz, REF: 8 kHz – 300 MHz.

Beta testing
Learning from users

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- More then 10 beta testers provided very relevant feedback on:
  - Position of switches and connectors
  - Presenting data on screen
  - Menu structure (advanced/basic menu)
  - Lack of robustness
  - Missing power meters
  - Regression testing
  - GPSDO locking speed to be improved.
  - Other performance problems
- Feedback included in SW and HW updates

Beta tester input example: Improving GPSDO locking speed

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- tinyGTC is a portable device allowing quick deployment
- GPSDO must reach frequency and/or phase lock as fast as possible also under non optimal conditions.
- Initial GPSDO:
  - One PID controller that after startup (very) slowly steers the frequency/phase.
  - Lock can take a long time
- Improved GPSDO:
  - Up to six separate controllers, either frequency or phase locked and each with own PID settings
  - Automatic selection of which controller to use for fast optimum accuracy under any given condition such as quality of GPS signal or temperature changes.

3rd HW model

(March 2025)

- Included all improvements
  - Different TDC's, more robust input switches, two power meters, flexible clock generator, charging IC away from TCXO
- All performance problems solved
- One design error (white wire)
- Robustness still not OK
  - Lifetime problem
- Connector spacing wrong
  - BNC adaptors won't fit

4th HW prototype

(July 2025)

- Improved connector spacing
- Performance difference between 1st and 4th HW models:

Spec	1st HW	4th HW
10 MHz ADEV at Tau = 1 s	1e-9	2e-12
Output frequencies	10 MHz	0.1 Hz to 100 MHz + 8 kHz to 100 MHz
Input frequencies	0.1 Hz to 80 MHz	0.1 Hz to 350 MHz Prescaler up to 7 or 12 GHz
Robustness	Switch with EMC problem during transport	1 hour 7 Vpp/20 dBm without problems
Power meter	N.A.	Both channels -25 dBm to + 20 dBm
Time resolution	40 ps	40 ps

Next steps

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- Performance good enough for product launch
- Small improvements still ongoing:
  - Remote control application (see demo)
- User documentation (WiKi) still to be extended.
- Instruction videos to be created
- Supply pipeline to be filled.
- Launch.

Learnings.

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- It is possible to build a counter with professional accuracy levels, even with cheap components, but this requires a lot of experience
  - The documented way is not always the right way
  - When looking with 40 ps resolution, everything is analog
  - Too much abstraction with HW creates problems
- For me, beta testers are indispensable
- The small form factor (handheld device) and low cost ambition made the design much more difficult.
  - Larger physical distances reduces coupling
  - Using LVDS for all clocks solves many problems
  - Separate input for GHz prescaler simplifies PCB design
- **Designing and evaluating a counter is an excellent long term learning opportunity**

Questions